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PATENT & TRADEMARK OFFICE

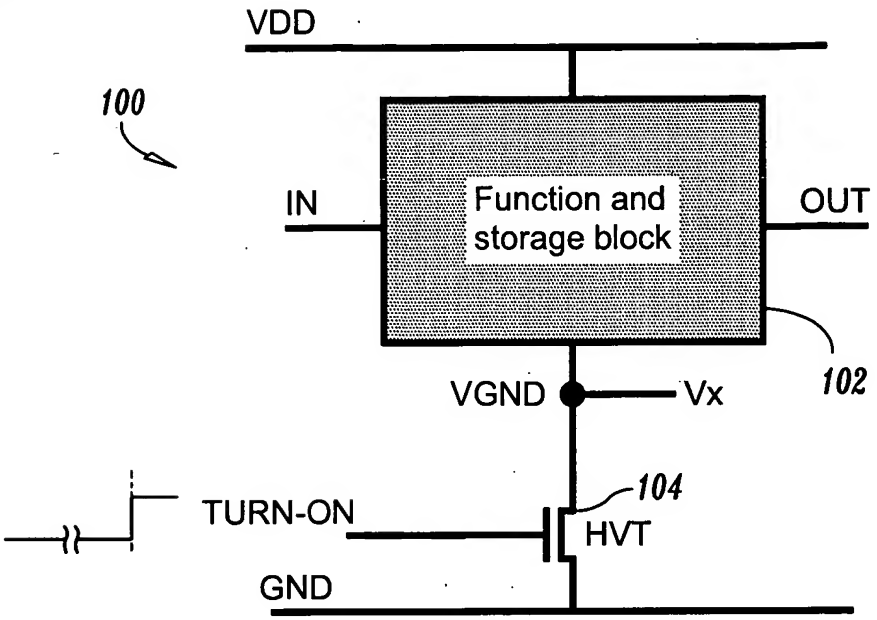

FIG. 1

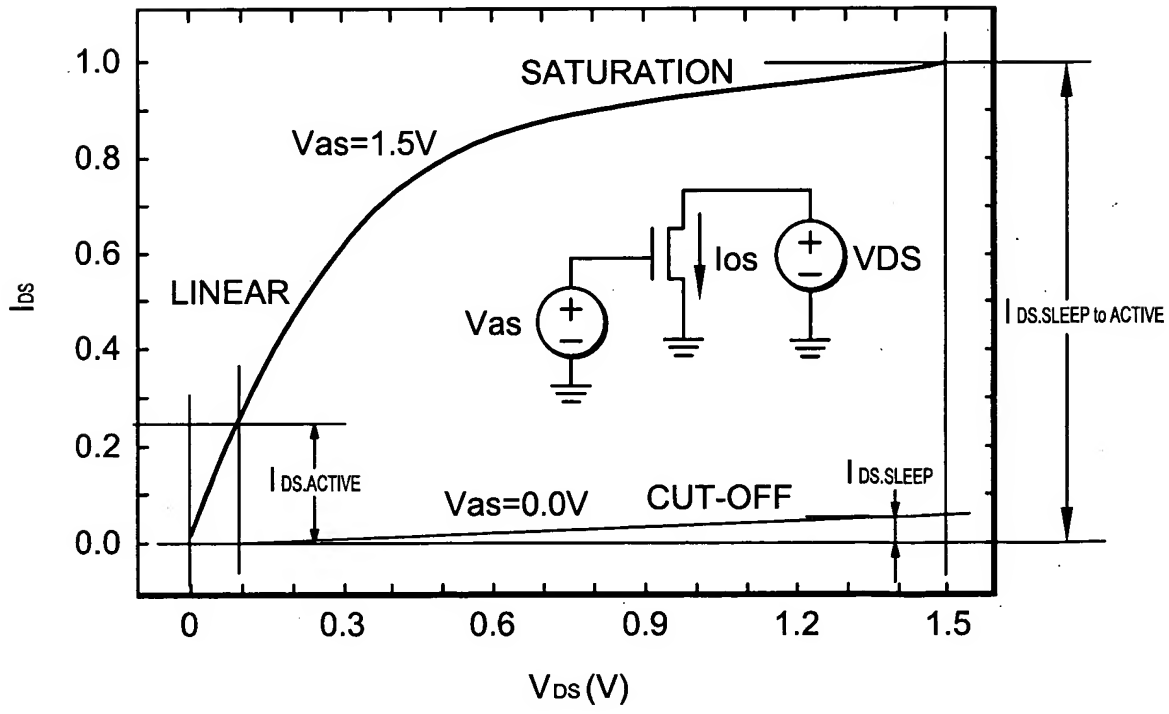

FIG. 2

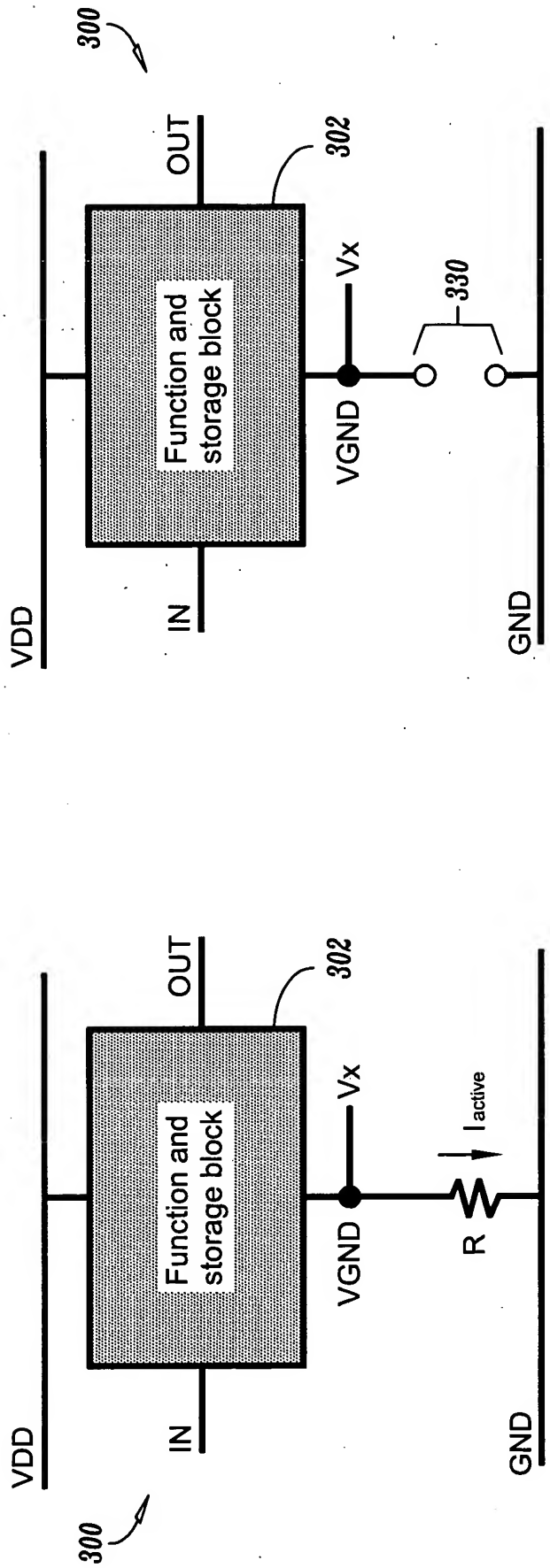

FIG. 3a

FIG. 3b

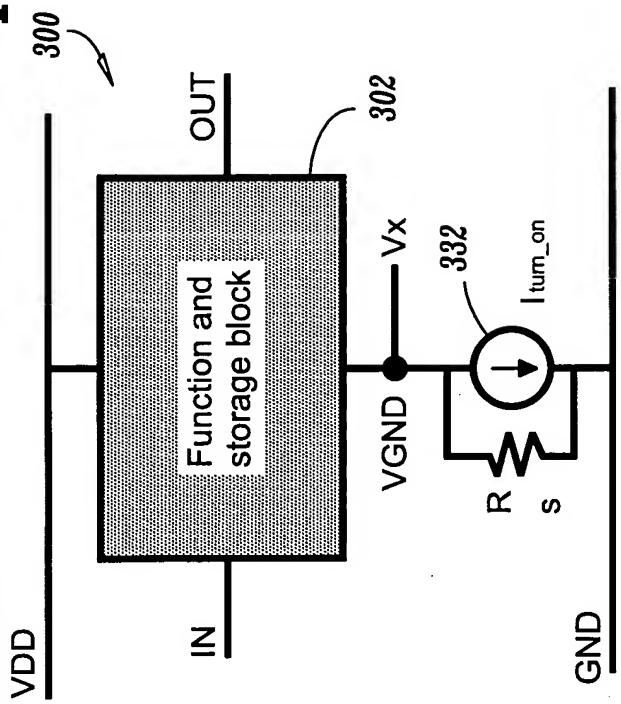

FIG. 3c

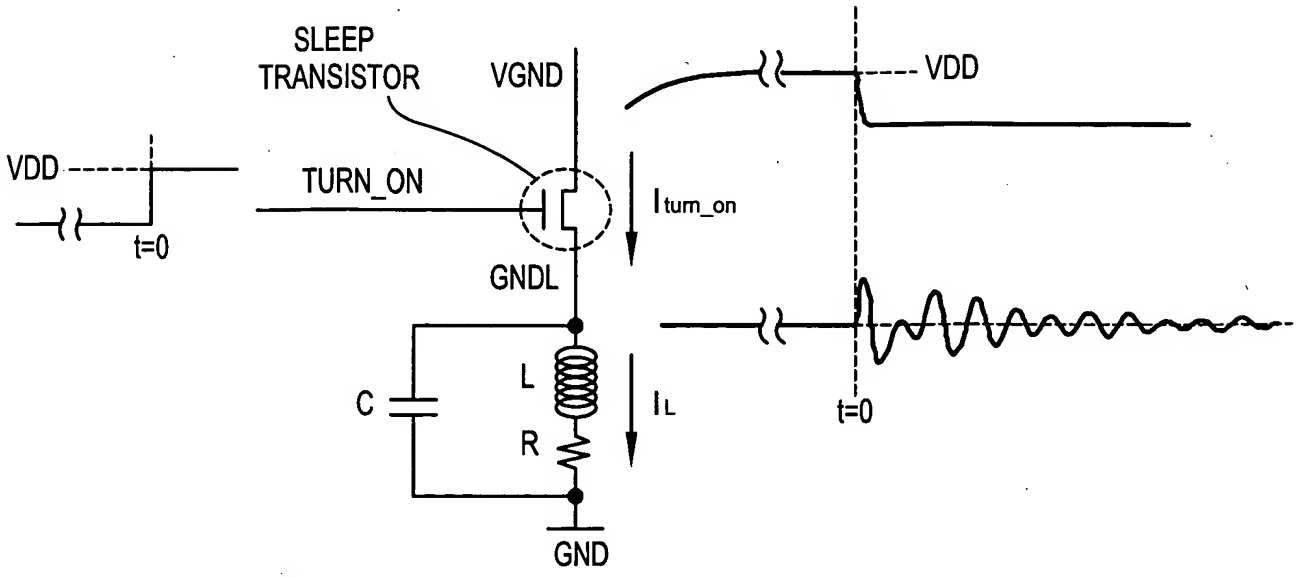
SLEEP
TRANSISTOR
VGND
VDD
VDD
TURN_ON
t=0
Iturn_on
GNDL
L
C
R
IL
t=0
GND

FIG. 4

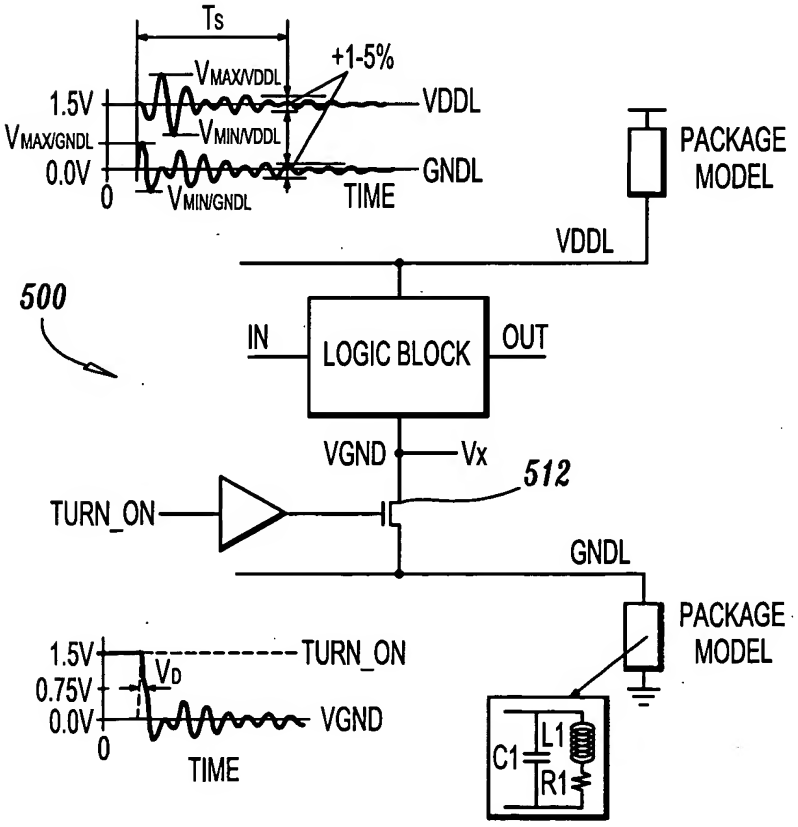
Ts
+1-5%
VMAX/VDDL
1.5V
VDDL
VMAX/GNDL
VMIN/VDDL
0.0V
GNDL
0
VMIN/GNDL
TIME
PACKAGE
MODEL
VDDL
500
IN
LOGIC BLOCK
OUT
VGND
Vx
512
TURN_ON
GNDL
PACKAGE
MODEL
1.5V
TURN_ON
VD
0.75V
0.0V
VGND
0
TIME
C1
L1
R1

FIG. 5

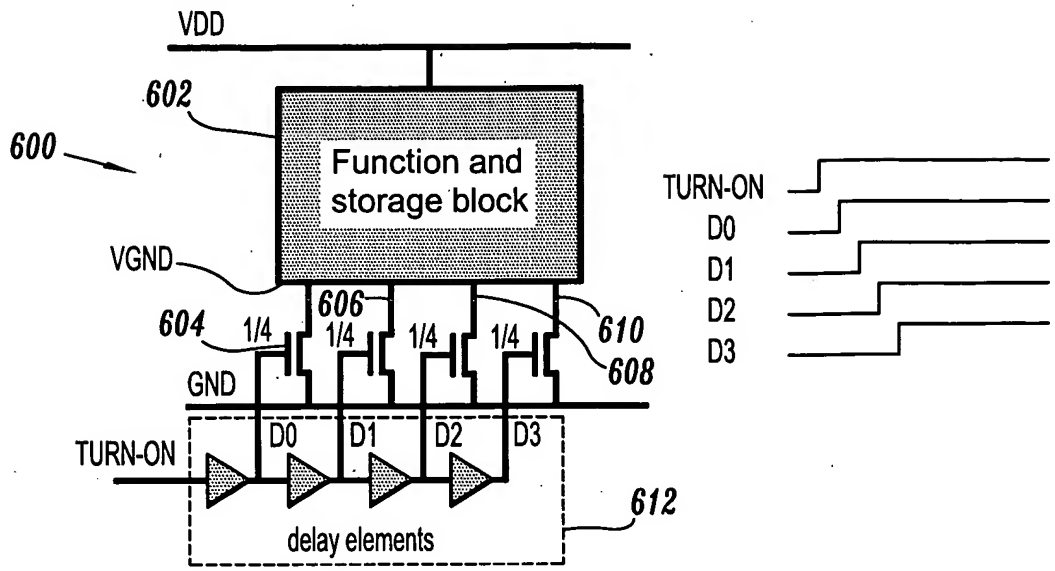

FIG. 6

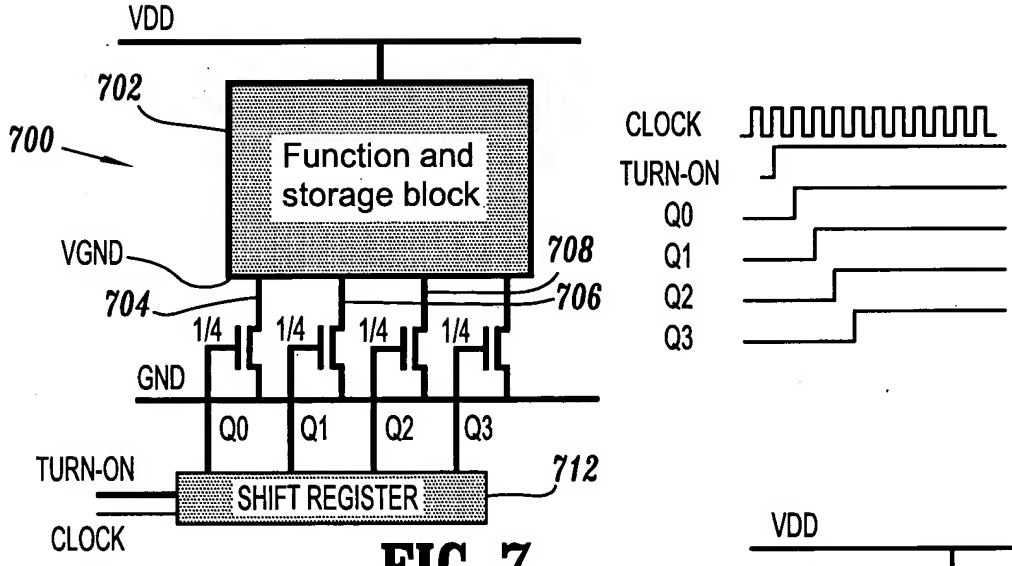

FIG. 7

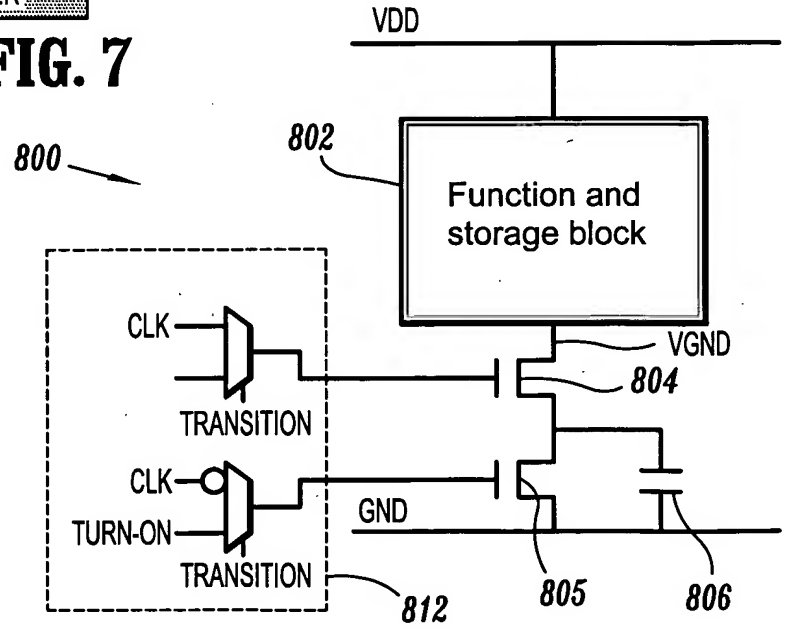

FIG. 8

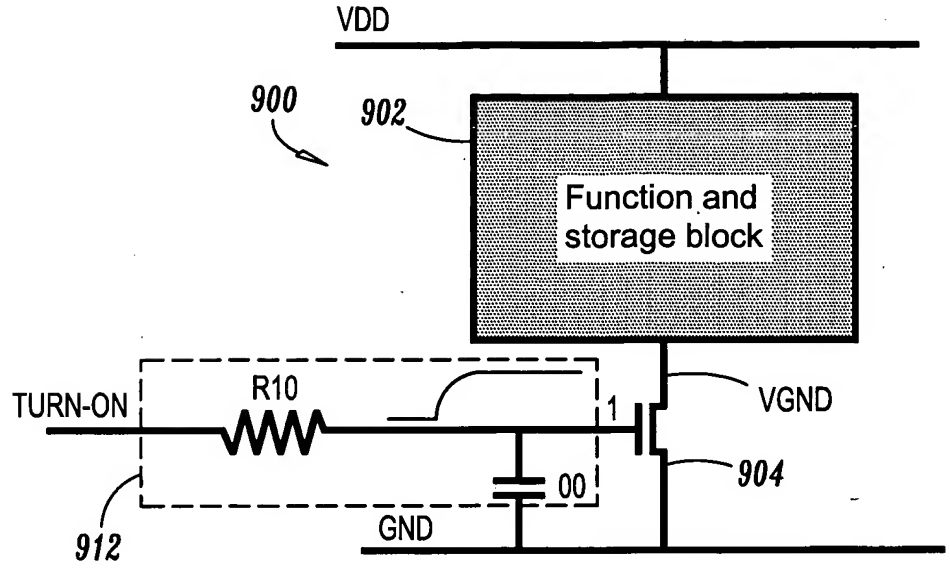
VDD
900
902
Function and storage block
TURN-ON
R10
1
VGND
904
00
GND
912

FIG. 9

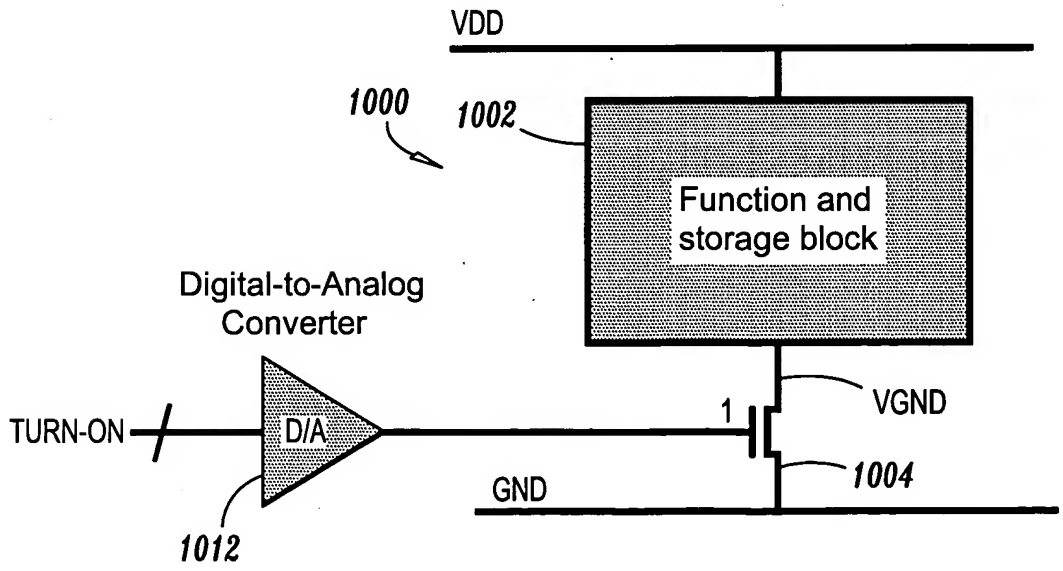
VDD
1000
1002
Function and storage block
Digital-to-Analog Converter
TURN-ON
D/A
1
VGND
1004
GND
1012

FIG. 10

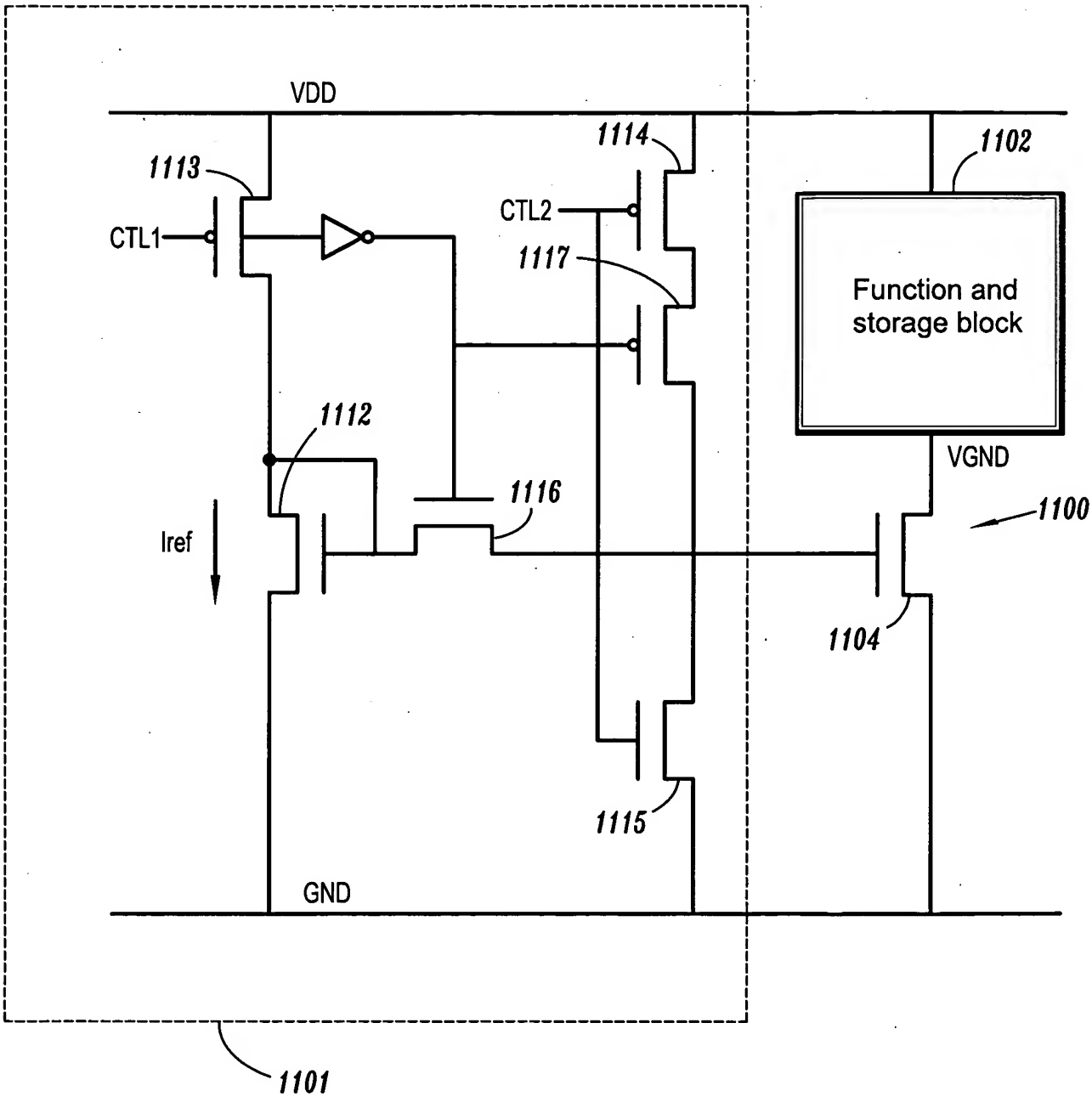
VDD
1113
CTL1
1114
CTL2
1117
1102
Function and storage block
1112
1116
VGND
1100
Iref
1104
1115
GND
1101

FIG. 11